What is Claimed is:

[c1] A semiconductor structure comprising:
an N+ diffusion and a P+ diffusion formed in a semiconductor substrate;
a polysilicon line formed on the substrate intersecting the N+ diffusion and the P+ diffusion;
wherein the polysilicon line has a P+ region, an N+ region and an N+/P+ junction area therebetween;
a silicide strap extending across the N+/P+ junction area of the polysilicon line wherein the silicide strap forms an electrical connection between the P+ region of the polysilicon line and the N+ region of the polysilicon line; and
wherein the N+ diffusion or the P+ diffusion are not silicided.

[c2] The semiconductor structure of claim 1, wherein the N+ diffusion is part of at least one NFET and wherein the P+ diffusion is part of at least one PFET.

[c3] The semiconductor structure of claim 1, wherein the semiconductor structure is part of an SRAM cell.

[c4] The semiconductor structure of claim 1, wherein the polysilicon line comprises at least one gate.

[c5] The semiconductor structure of claim 1 wherein current leakage in the semiconductor structure is reduced by preventing silicide formation on the N+ diffusion and the P+ diffusion.

[c6] The method of claim 5 wherein the current leakage reduced comprises Gate Induced Drain Leakage (GIDL).

[c7] A semiconductor device comprising:
a first PFET, the first PFET including a source diffusion and a drain diffusion;
a first NFET, the first NFET including a source diffusion and a drain diffusion;
a first polysilicon line connecting the first NFET to the first PFET, the first polysilicon line including a N+ portion, a P+ portion and a N+/P+ junction area; and
a silicide strap extending across the N+/P+ junction area of the first polysilicon line wherein the silicide strap forms an electrical connection between the P+ portion and the N+ portion of the first polysilicon line, and wherein the silicide strap is not formed on

the PFET source diffusion and PFET drain diffusion and wherein the silicide strap is not formed on the NFET source diffusion and NFET drain diffusion.

[c8] The semiconductor device of claim 7 further comprising:
a second PFET, the second PFET including a source diffusion and a drain diffusion;
a second NFET, the second NFET including a source diffusion and a drain diffusion;
a second polysilicon line connecting the second NFET to the second PFET, the second polysilicon line including a N+ portion, a P+ portion and a N+/P+ junction area; and
a second silicide strap extending across the N+/P+ junction area of the second polysilicon line wherein the silicide strap forms an electrical connection between the P+ portion and the N+ portion of the second polysilicon line, and wherein the second silicide strap is not formed on the PFET source diffusion and PFET drain diffusion and wherein the second silicide strap is not formed on the NFET source diffusion and NFET drain diffusion.

[c9] The semiconductor device of claim 7 wherein the first PFET and the first NFET are portions of an SRAM device.

[c10] The semiconductor device of claim 7, wherein the first polysilicon line comprises a gate of the first PFET and the first NFET.

[c11] The semiconductor device of claim 8, wherein the second PFET and the second NFET are portions of an SRAM device.

[c12] The semiconductor device of claim 8, wherein the second polysilicon line comprises a gate of the second PFET and the second NFET.

[c13] The semiconductor structure of claim 7 wherein current leakage is reduced by preventing silicide formation on the PFET source diffusion and PFET drain diffusion and the NFET source diffusion and NFET drain diffusion.

[c14] The semiconductor structure of claim 13 wherein the current leakage reduced comprises Gate Induced Drain Leakage (GIDL).

[c15] The semiconductor structure of claim 8 wherein current leakage is reduced by preventing silicide formation on the PFET source diffusion and PFET drain diffusion and the NFET source diffusion and NFET drain diffusion.

[c16] The semiconductor structure of claim 15 wherein the current leakage reduced comprises Gate Induced Drain Leakage (GIDL).

[c17] A method for forming a semiconductor apparatus comprising the steps of:
forming an N+ diffusion and a P+ diffusion;
forming a polysilicon line, the polysilicon line having a P+ region and an N+ region, the polysilicon line having an N+/P+ junction area wherein said junction area comprises the area where the P+ region of the polysilicon line and the N+ region of the polysilicon line abut each other; and,
selectively forming a silicide strap extending across the junction area, wherein the silicide strap forms an electrical connection between the P+ region of the polysilicon line and the N+ region of the polysilicon line; and
selectively preventing the formation of silicide on the N+ diffusion and the P+ diffusion.

[c18] The method of claim 17 wherein the step of selectively forming a silicide strap comprises:
forming a hard mask on the semiconductor structure;
patterning the hard mask to expose the N+/P+ junction area; and
forming silicide in the exposed N+/P+ junction area.

[c19] The method of claim 17 wherein the step of selectively preventing the formation of silicide on the N+ diffusion and the P+ diffusion comprises:
forming a hard mask on the semiconductor structure; and
patterning the hard mask to expose portions of the semiconductor structure, said patterning not exposing the N+ diffusion and the P+ diffusion.

[c20] The method of claim 17 further comprising the step of:
completing devices and back end of line processes.

[c21] The method of claim 17 wherein the semiconductor structure is part of an SRAM.

[c22] The method of claim 17 wherein current leakage is reduced by selectively preventing silicide formation on the N+ diffusion and P+ diffusion.

[c23] The method of claim 22 wherein the current leakage reduced comprises Gate Induced Drain Leakage (GIDL).